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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,754	01/17/2002	Masaki Okuda	107337-00006	2642

7590 11/04/2004

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,754	OKUDA, MASAKI	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 19 April 2004 was filed after the mailing date of the application on 27 January 2002. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

The application remains in non-final status since after further consideration of applicant's claimed invention in view of applicant's remarks; the examiner has determined claims 2, 4 and 8 do not contain allowable subject matter. As such, the examiner has rescinded his objection of claims 2, 4 and 8 as being dependent upon a rejected base claim but would be allowable if independent form. Therefore the application remains non-final to provide the applicant with an opportunity to respond to examiner's new grounds for rejection.

In the prior office action, the examiner used the claim language of Yagishita et al., US Patent 6,529,435 ('435) claim 1 and Kitamoto et al., US Patent 6,421,292 ('292) claim 1. Since this leads to confusion over which patent forms the basis of rejection under the doctrine of obviousness-type double patenting, the examiner has restructured his rejection such that claim 1 of '435 is the basis of rejection and the disclosure of '292 as the grounds of obviousness. Since '292's discloses the limitations under contention,

which have been incorporated into the examiner's rejection, the applicant's remarks are moot.

As such, the examiner respectfully maintains his rejection of claims 1-6 and 8 under the doctrine of obviousness-type double patenting based upon '435 in view of '292.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-6 and 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of US Patent 6,529,435 ('435) in view of U.S. Patent No. 6,421,292 ('292).

In regards to claim 1,

a refreshing circuit for refreshing said memory is claimed in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is claimed in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is claimed in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is claimed in '435 claim 1 lines 5-8;

'435 does not claim:

a data inputting circuit for receiving data inputted from an external circuit,

a parity generating circuit for generating parity data from the data input from said data inputting circuit,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit,

or a parity outputting circuit for directly reading and outputting the parity data.

'292 shows:

a data inputting circuit for receiving data inputted from an external circuit in figure 15 element 115,

a parity generating circuit for generating parity data from the data input from said data inputting circuit in figure 15 element 106,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit in figure 15 element 108 receiving and storing data from element 115 and 106,

and a parity outputting circuit for directly reading and outputting parity data in figure 15 element 107.

'435 and '292 both use parity to generate data when a read is received during a refresh operation. '435 is primarily concerned with the exact method of storing data and parity into the memory and the means for accessing information when the memory is under a refresh operation. '435 implements the memory outlined in '292 (compare figure 1 of '435 and figure 16 of 292, the internal structure of the memory cells are *identical*) with logic necessary to interface with external signals in a computer environment. Since it is clear that '292 builds upon concepts disclosed in '435, it would have been obvious to one of ordinary skill in the art to incorporate the interface circuitry discloses in '292 in '435.

In regards to claim 2, '292 shows said parity outputting circuit outputs the parity data via a terminal which is the same as a terminal through which said data outputting circuit outputs data in figure 15 element 107 in connection with element 115.

In regards to claim 3,

a refreshing circuit for refreshing said memory is claimed in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is claimed in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is claimed in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is claimed in '435 claim 1 lines 5-8;

'435 does not claim:

a data inputting circuit for receiving data inputted from an external circuit,

a parity generating circuit for generating parity data from the data input from said data inputting circuit,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit,

or a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity is stored.

'292 shows:

a data inputting circuit for receiving data inputted from an external circuit in figure 15 element 115,

a parity generating circuit for generating parity data from the data input from said data inputting circuit in figure 15 element 106,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit in figure 15 element 108 receiving and storing data from element 115 and 106,

and a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity is stored in figure 15 wdata signal line feeding element 182.

'435 and '292 both use parity to generate data when a read is received during a refresh operation. '435 is primarily concerned with the exact method of storing data and parity into the memory and the means for accessing information when the memory is under a refresh operation. '435 implements the memory outlined in '292 (compare figure 1 of '435 and figure 16 of 292, the internal structure of the memory cells are *identical*) with logic necessary to interface with external signals in a computer environment. Since it is clear that '292 builds upon concepts disclosed in '435, it would have been obvious to one of ordinary skill in the art to incorporate the interface circuitry discloses in '292 in '435.

In regards to claim 4, '292 shows said writing circuit inputs said desired data via a terminal in which is the same as a terminal through which data inputting circuit inputs data in figure 15 element 115's interface with the external data.

In regards to claim 5, '292 shows a parity outputting circuit for directly reading and outputting the parity data stored in said memory in figure 15 element 107.

In regards to claim 6,

a refreshing circuit for refreshing said memory is claimed in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is claimed in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is claimed in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is claimed in '435 claim 1 lines 5-8;

'435 does not claim:

a data inputting circuit for receiving data inputted from an external circuit,

a parity generating circuit for generating parity data from the data input from said data inputting circuit,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit,

a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored,

or a control circuit for controlling said refreshing circuit to refresh circuit to refresh a given area according to a request from an external circuit; and said control circuit controls said refreshing circuit to refresh an area specified by the external circuit.

'292 shows:

a data inputting circuit for receiving data inputted from an external circuit in figure 15 element 115,

a parity generating circuit for generating parity data from the data input from said data inputting circuit in figure 15 element 106,

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit in figure 15 element 108 receiving and storing data from element 115 and 106,

a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored in figure 15 wdata signal line feeding element 182,

and a control circuit for controlling said refreshing circuit to refresh circuit to refresh a given area according to a request from an external circuit; and said control circuit controls said refreshing circuit to refresh an area specified by the external circuit

in column 1 lines 14-17. While this feature is disclosed in the background and '292 specifies an internally triggered refresh, the accessing of a memory array during a refresh operation via parity blocks and the internally generated refresh signal are separable and distinct features of '292. Neither feature is necessary for the operation of the other. '292 states in the background (column 1 lines 14-17) that the refreshing of a memory is conventionally performed by external means. Since the two aforementioned features are separable and '292 states that refreshing memory by external means is well known in the art, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate an external refresh means with accessing memory during a refresh operation using parity blocks.

'435 and '292 both use parity to generate data when a read is received during a refresh operation. '435 is primarily concerned with the exact method of storing data and parity into the memory and the means for accessing information when the memory is under a refresh operation. '435 implements the memory outlined in '292 (compare figure 1 of '435 and figure 16 of 292, the internal structure of the memory cells are *identical*) with logic necessary to interface with external signals in a computer environment. Since it is clear that '292 builds upon concepts disclosed in '435, it would have been obvious to one of ordinary skill in the art to incorporate the interface circuitry discloses in '292 in '435.

In regards to claim 8, '435 shows said control circuit controls said refreshing circuit to refresh an area specified, and said data outputting circuit outputs data read from area to be refreshed and restored based on parity data claim 1 lines 23-28.

The limitation "a control circuit for controlling said refreshing circuit to refresh circuit to refresh a given area according to a request from an external circuit; and said control circuit controls said refreshing circuit to refresh an area specified by the external circuit" was rejected in the parent claim, please refer to the rejection of claim 6 for the rejection and motivation for rejection.

Allowable Subject Matter

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (571)272-24203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan 11/1/04

PB

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER